IN THE CLAIMS

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1. (Previously Presented) A microelectronic package, comprising:

a planar heat sink;

more than one microelectronic die, each having an active surface and a back surface, said more than one microelectronic die back surface adjacent to said heat sink;

a patterned thermally conductive adhesive layer disposed between said more than one microelectronic die and said heat sink; and

an encapsulation material disposed on said heat sink and said microelectronic die active surface.

2. (Original) The microelectronic package of claim 1, further including a build-up layer disposed on an upper surface of said encapsulation material.

3. (Previously Presented) The microelectronic package of claim 2, wherein said build-up layer comprises at least one conductive trace disposed on said encapsulation material upper surface, wherein a portion of said at least one conductive trace extending through said encapsulation material to contact at least one microelectronic die active surface.

4. (Original) The microelectronic package of claim 3, wherein said build-up layer further includes at least one dielectric layer disposed on at least a portion of the encapsulation material upper surface and said at least one conductive trace, and at least one second conductive trace extending through said at least one dielectric layer to contact said at least one conductive trace.

Claims 5-9 (Canceled)

10. (Previously Presented) A microelectronic package, comprising:

a planar heat sink;

a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface, where said microelectronic package core second surface abuts said planar heat sink;

more than one microelectronic die disposed within said at least one microelectronic package core opening and adjacent said planar heat sink, each said more than one microelectronic die having an active surface; and

an encapsulation material disposed on said microelectronic die and in portions of at least one microelectronic package core opening.

11. (Original) The microelectronic package of claim 10, further including a build-up layer disposed on an upper surface of said encapsulation material.

12. (Previously Presented) The microelectronic package of claim 11, wherein said build-up layer comprises at least one conductive trace disposed on said encapsulation material upper surface, wherein a portion of said at least one conductive trace extends through said encapsulation material to contact at least one microelectronic die active surface.

13. (Original) The microelectronic package of claim 12, wherein said build-up layer further includes at least one dielectric layer disposed on at least a portion of the encapsulation material upper surface and said at least one conductive trace, and at least one second conductive trace extending through said at least one dielectric layer to contact said at least one conductive trace.

14. (Original) The microelectronic package of claim 11, wherein said encapsulation material covers said microelectronic package core first surface.

15. (Previously Presented) The microelectronic package of claim 10, wherein a thickness of said microelectronic package core is greater than a thickness of said more than one microelectronic die.

16. (Original) The microelectronic package of claim 10, wherein said microelectronic package core is a material selected from the group consisting of bismaleimide triazine resin based material, an FR4 material, polyimides, ceramics, and metals.

17. (Previously Presented) The microelectronic package of claim 10, further including a thermally conductive adhesive layer disposed between said at least one microelectronic die and said planar heat sink.

Claims 18-28 (Canceled)

29. (Previously Presented) The microelectronic package of claim 1, further including:

a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface, where said microelectronic package core second surface abuts said planar heat sink; and

wherein the more than one microelectronic die is disposed within said at least one microelectronic package core opening and adjacent said heat sink, each said more than one microelectronic die having an active surface, and a patterned thermally conductive adhesive layer disposed between said more than one microelectronic die and said planar heat sink.